Hysteresis current control with distributed shoot-through states for impedance source inverters

Oleksandr Husev1,2, Andrii Chub1,*, Enrique Romero-Cadaval3, Carlos Roncero-Clemente3 and Dmitri Vinnikov4

1Department of Electrical Engineering, Tallinn University of Technology, Tallinn, Estonia
2Department of Biomedical Radioelectronics Apparatus and Systems, Chernihiv National Technological University, Chernihiv, Ukraine
3School of Industrial Engineering, University of Extremadura, Badajoz, Spain
4Institute of Industrial Electronics and Electrical Engineering, Riga Technical University, Riga, Latvia

SUMMARY

This paper presents a hysteresis current control technique with shoot-through states distribution. This control algorithm could be applied to three-level and multi-level inverters with any impedance source network where reference current control signal along with shoot-through states are required. Possible modifications of the presented algorithm are discussed. The steady-state analysis was made to explain the operation principle of the algorithm. As a result, the link between the band ratio of the hysteresis current controller, the input voltage, and the desired DC-link voltage was obtained. All theoretical predictions were proved by simulation and experimental results. Future applications are discussed.

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1. INTRODUCTION

Renewable energy sources have become extremely popular. As a result, many new types of interface converters have emerged. The family of the single-stage buck boost inverters based on Z-source (ZS) network or any other Z-source-derived network (Figure 1) is highlighted.

The ZS network proposed in [1] can overcome main drawbacks of the voltage source inverter and the current source inverter (CSI). The main merit of this topology is the buck-boost operation capability. Voltage regulation within a single-stage inverter is achieved by means of cross conduction of transistors – shoot-through switching states. Many other new impedance source (IS) networks have been proposed recently. Figure 2 shows some of those networks. The quasi-Z-source (qZS) inverter topology proposed in [2] has continuous input current, which is preferable in renewable energy applications [3–5].

In the further development, it was intended to extend the regulation capability by means of coupled inductors whose turn ratios can be different. A trans-Z-source (or T-source; TZS) network was proposed in [6–8]. Extended voltage gain and reduced element count are the main advantages of the TZS network over the ZS and qZS networks.

*Correspondence to: Andrii Chub, Department of Electrical Engineering, Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia.
†E-mail: andrii.chub@ttu.ee

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The trans-quasi-Z-source (TQZS) network shown in Figure 2(d) is a variant of the TZS. As compared with the TZS, double-reduced capacitance of the TQZS with a unity turns ratio can be achieved. However, after capacitance replacing, the shape of the input current will worsen, and a discontinuous input current is introduced [9]. Many other topologies are available to increase the gain factor [10–15], the TZS network being among them [14]. Logical deviation of an inductor’s coupling idea occurred in the Y-source network (Figure 2(f)). Turns ratio and winding placement of the three-winding inductor can be designed to achieve the desired gain, while maintaining a small switch duty ratio [15].

The IS networks described previously have been demonstrated for DC–AC, DC–DC, and AC–AC applications [16, 17]. Such new generation of DC–DC converters with single-stage energy conversion can realize grid connection along with the maximum power point tracking function with a wider input voltage range operation than in conventional inverter topologies. Traditionally, modulation techniques for IS inverters with boost control are used in similar applications [18–23]. The classification is summarized in Figure 3.

For instance, maximum boost control was proposed in [16]. The main drawback of that approach is the low-frequency input current ripple. Maximum constant boost control solves the problem by using the constant shoot-through duty ratio along with the third harmonic injection [19]. Typically, a three-phase system is discussed, but all of them can be modified for single-phase applications as well as for multilevel inverter topologies [23–27].

Further, many special space vector modulation techniques with embedded shoot-through duty cycle have been developed [28–30]. The main drawback of such solutions is the high demands to the control system. As a result, industrial applications are limited [31].
Hysteresis current control, which is based on the current reference signal, is often used in traditional CSI and voltage source inverter solutions [32–37]. In addition, several approaches for multilevel converters are described in [38, 39]. Commonly, hysteresis control is preferable because of simplicity, fast deadbeat transient response, and overcurrent protection. But it is difficult to implement it in the system with shoot-through states.

This paper proposes a novel hysteresis current control for a single-phase inverter based on any IS network with distributed shoot-through states. Section 2 explains the novel algorithm in detail. The steady-state analysis is presented in Section 3. Section 4 describes the simulation along with experimental results. Finally, conclusions are presented in Section 5. This paper is based on earlier preliminary publication [40] and includes a comprehensive theoretical analysis and experimental results; however, it is not presented there.

2. NEW HYSTERESIS CURRENT CONTROL METHODS

2.1. Novel simple hysteresis current control

The novel hysteresis control is outlined in Figure 4(a). The main idea is to use a modified hysteresis control with shoot-through states distribution. Total hysteresis current band ΔI defines the current error and includes a main band ΔI₀ (Figure 4(c)) and an auxiliary shoot-through current band ΔIₛ. The control system requires a reference grid current iₙ at the input.

When the grid current iₙ reaches the upper current limit (point a in Figure 4(b) and (c)), the zero state is switched on, and the grid current starts falling.

At the instant when the grid current crosses the boundary line between ΔI₀ and ΔIₛ (point b), the shoot-through state appears. In point c, the grid current reaches a lower limit, and the active state is switched on up to point d.

The band ratio between the auxiliary band ΔIₛ and the total band ΔI defines the necessary boost factor. Figure 4(c) shows the time diagram of the single switching cycle upon an assumption that the reference current remains constant in a switching cycle.

2.2. Modified hysteresis control methods

Figure 5 illustrates several modified hysteresis control methods. The first idea lies in the modulation of hysteresis bands. Figure 5(a) shows this principle with sinusoidal modulation.

Typically, the switching frequency is higher near zero crossing points where the derivative of the reference current waveform has maximum value and higher waveform distortion. The aim of such
modification is to decrease the total harmonic distortion (THD) of the current and to smoothen switching losses. Although the switching frequency is even higher near zero current value, switching losses are minor. It should be noted that many other modification possibilities based on the hysteresis band modulation exist [29–33].

Figure 5(b) illustrates a multilevel application possibility of the proposed hysteresis approach. The corresponding states are defined by the region where current is detected. The idea of such approach is to separate the active states into several levels in accordance with the number of converter levels.
In the three-level (3L) topology, in the time domain of the half cycle from 0 to $\gamma$ and from $\pi - \gamma$ to $\pi$, half of the DC-link voltage $V_{DC}$ is applied. In the complementary time domain from $\gamma$ to $\pi - \gamma$, full DC-link voltage is applied. Such approach can be generalized and applied for any N-level topology.

Further analysis was made considering an L-filter at the output. However, the high-order grid side filters, like LCL-filter, are common in high-power applications to satisfy power quality standards and ensure acceptable power density. A combination of a high-order filter and the hysteresis control can lead to an unstable operation [41]. Undesirable resonance in the grid side filter can be suppressed with active and passive damping [42]. Active damping shows good performance in systems with a hysteresis current controller and an LCL-filter [43], while the control system design with active damping requires a complicated analysis [44]. Passive damping approach is the simplest solution for filter stabilization, while it employs additional passive network with resistors, which results in higher losses [45]. A digital hysteresis control system can also improve stability of the IS inverter at constant switching frequency, which limits the output current spectrum [46].

Another issue that could limit the performance of the proposed control system is an inherent instability of the IS inverters. Operation of the IS inverters changes significantly at transition between the continuous and the discontinuous conduction modes (DCM) [47]. The IS network usually contains inductors and capacitors, which leads to the non-minimum phase dynamic behavior and the presence

Figure 5. Modified hysteresis control method: basic principle (a) and example of control of 2L (when $\gamma=0$) and 3L inverters (b).
of resonance frequencies [48, 49]. However, in practice, the influence of these factors can be mitigated with passive damping, limited switching frequency range, or improved two-loop control [50].

3. STEADY-STATE ANALYSIS OF THE PROPOSED METHODS

To define the correlation between band ratios and boost properties, the steady-state analysis was made. For a generalization, the three-level topology in this analysis is discussed. It is easy to proceed to the two-level (2L) inverter assuming $\gamma=0$.

A general equation that describes the behavior of the grid current during the time interval $t_0 - t_1$ and $t_1 - t_2$ (Figure 4(c))

$$L_g \frac{dI_g(t)}{dt} = V_{inv}(t) - V_g = V_{inv}(t) - V_M \sin(\omega t) ,$$

where $V_M$ is the amplitude of the grid phase-to-neutral voltage and $V_{inv}(t)$ is the instantaneous output voltage of the inverter.

Time interval $t_0 - t_1$ corresponds to the zero state and $t_1 - t_2$ to the shoot-through state where $V_{inv}(t)=0$ and assuming that the minimum switching frequency is well over the grid frequency, as a result, the time interval can be estimated as

$$t_2 - t_0 = \frac{\Delta I(t) \cdot L_g}{V_M \sin(\omega t)} ,$$

where $\Delta I(t)=\alpha \cdot I_g(t)$.

A general equation that describes the behavior of the grid current during the active state in the time interval $t_2 - t_3$

$$L_g \frac{dI_g(t)}{dt} = \tilde{V}_{inv}(t) - V_M \sin(\omega t) ,$$

where $\tilde{V}_{inv}(t)$ is the instantaneous peak value of the inverter output voltage. It equals either $V_{DC}/2$ or $V_{DC}$ for a positive half wave. The function in a phase domain for a positive half wave of the current, as shown in Figure 5(b) can be defined as

$$\tilde{V}_{inv}(\omega t) = \begin{cases} V_{DC}/2, & \text{if } 0 \leq \omega t \leq \gamma \text{ or } \pi - \gamma \leq \omega t \leq \pi, \\ V_{DC}, & \text{if } \gamma \leq \omega t \leq \pi - \gamma. \end{cases}$$

Similarly, the time interval can be estimated as

$$t_3-t_2 = \frac{\Delta I(t) \cdot L_g}{(\tilde{V}_{inv}(t) - V_M \sin(\omega t))} .$$

From the equations previously mentioned, it is possible to obtain the shoot-through duty ratio for the single switching cycle:

$$d_S = \frac{(t_2-t_1)}{(t_3-t_0)} .$$

In Figure 4(c), the ratio between the time intervals can be defined as

$$t_2-t_1 = (t_2-t_0) \frac{\Delta I_S}{\Delta I} = (t_2-t_0) \cdot \Delta_S ,$$

where $\Delta_S=\Delta I_S/\Delta I$ is an auxiliary band ratio. The shoot-through duty ratio can be expressed as
\[ d_S(t) = \Delta_S \left(1 - \frac{V_M \sin (\omega t)}{V_{\text{inv}}(t)}\right). \] (8)

An average value of the shoot-through duty cycle can be calculated as (integrating in a phase domain, where \( \omega t = \phi \), over a half fundamental period)

\[
D_S = \frac{1}{\pi} \int_0^\pi d_S(\phi) d\phi
= \frac{1}{\pi} \int_0^\pi \Delta_S \left(1 - \frac{V_M \sin(\phi)}{V_{\text{inv}}(\phi)}\right) d\phi
= \frac{1}{\pi} \left[2 \int_0^\gamma \Delta_S \left(1 - \frac{2V_M \sin(\phi)}{V_{DC}}\right) d\phi + \int_\gamma^{\pi - \gamma} \Delta_S \left(1 - \frac{V_M \sin(\phi)}{V_{DC}}\right) d\phi\right]
= \Delta_S \left(1 - \frac{4V_M}{\pi V_{DC}} \left(1 - \frac{1}{2} \cos(\gamma)\right)\right). \] (9)

From previous studies [1–4], it can be concluded that constant output voltage is achieved by maintaining the constant capacitance voltage \( (C_1 \text{ in Figure 2}) \):

\[ V_C = V_{IN} \frac{1 - D_S}{1 - 2D_S}, \] (10)

while the DC-link voltage strictly depends on the input voltage:

\[ V_{DC} = 2V_C - V_{IN}. \] (11)

Substituting Eqs. (10) and (11) into Eq. (9), the expression that links the input voltage \( V_{IN} \), the auxiliary band ratio \( \Delta_S \), the angle \( \gamma \), and the capacitor voltage \( V_C \) all together can be obtained as

\[ \Delta_S = \frac{V_C - V_{IN}}{2V_C - V_{IN} - \frac{2}{\pi} V_M (2 - \cos(\gamma))}. \] (12)

Figure 6 illustrates the dependences of the auxiliary band ratio \( \Delta_S \) versus the input voltage \( V_{IN} \), while the capacitor voltage \( V_C \) remains constant and equal to the amplitude of the grid voltage \( V_M \). Angle \( \gamma = 0 \), which corresponds to the two-level topology. The maximum value of the auxiliary band ratio corresponds to the minimum value of the input voltage. \( \Delta_S = 1 \) corresponds to the minimum possible value of the input voltage with maximum DC-link utilization. In the 3L topology (dotted line), an increase in the angle \( \gamma \) leads to a decrease in the input voltage operation range. The benefit of the 3L topology is the quality of the output current.

Controlling the capacitor voltage is a relatively simple approach. But at the same time, from Eq. (11), it is evident that the DC-link will vary in a wide range similar to the maximum constant boost control in [19]. As compared with hysteresis control, the capability of DC-link use in most carrier-based controls is worse.

To achieve maximum performance of DC-link use, we will find dependences between the auxiliary band ratio \( \Delta_S \), the input voltage \( V_{IN} \), and the DC-link voltage \( V_{DC} \).
In most cases, in the impedance topologies described previously, the boost factor is

\[ B = \frac{V_{DC}}{V_{IN}} = \frac{1}{1 - 2D_S}. \] (13)

Taking into account Eq. (13), auxiliary band ratio \( \Delta_S \) dependences can be expressed from Eq. (9) as a function of the input voltage, the desired DC-link voltage and the angle of the applied voltage of the converter:

\[ \Delta_S = \frac{\Delta I_S}{\Delta I} = \frac{V_{DC} - V_{IN}}{2\left(V_{DC} - \frac{1}{2}V_M'\left(1 - \frac{1}{2}\cos(\gamma)\right)\right)}. \] (14)

Figure 7 illustrates the dependences of the auxiliary band ratio \( \Delta_S \) versus the input voltage \( V_{IN} \), while the DC-link voltage remains constant. Figure 7(a) shows several curves with different DC-link voltages and the angle \( \gamma = 0 \), which corresponds to the 2L topology. The maximum value of the auxiliary band ratio corresponds to the minimum value of the input voltage. \( \Delta_S = 1 \) corresponds to the minimum possible value of the input voltage with maximum DC-link utilization. It should be noted that the rise of the DC-link voltage leads to a decrease in the required auxiliary band ratio \( \Delta_S \) in a steady-state mode. It means that when current rise up time shrinks while current fall down time remains the same.

In the 3L topology, as can be seen, an increasing angle \( \gamma \) leads to a decreasing input voltage operation range. The benefit of the 3L topology is the quality of the output current. This phenomenon is demonstrated in Figure 7(b).

Figure 7(b) enables us to predict that an optimal dependence between the auxiliary band ratio \( \Delta_S \) and the input voltage \( V_{IN} \) with maximum DC-link utilizing performance exists. The minimum value of \( V_{DC} \) for each \( V_{IN} \) can be found. When \( V_{IN} \) is very low, the highest value of the auxiliary band ratio (\( \Delta_S = 1 \)) can maintain the required boost level. From (14), that curve can be derived analytically. On the other hand, minimum DC-link voltage is limited by the amplitude of the grid voltage.

Figure 8 illustrates the reasoning presented previously. In the first region, \( \Delta_S = 1 \) and \( V_{DC} \) declines from a maximum value to \( V_M \). In the second region, \( V_{DC} = V_M \) and \( \Delta_S \) is decreasing from 1 to 0. Both regions correspond to the boost mode. Finally, the third region meets classical hysteresis control in the buck mode.
Figure 7. Boost capability of the proposed hysteresis control approach with different parameters: $\gamma = 0$ (a), $\gamma = \pi/6$ (b).

Figure 8. Voltage boost capability of the proposed hysteresis control approach with different parameters: $\gamma = 0$ (a), $\gamma = \pi/6$ (b).
4. SIMULATION AND EXPERIMENTAL FEASIBILITY STUDY OF THE PROPOSED HYSTERESIS METHODS

To verify all theoretical predictions, several simulations and experimental tests were carried out. Figure 9 shows the case study system. The ZS and qZS networks with an H-bridge inverter were chosen for the simulation study with synchronous sampling. Passive elements are the same for both cases.

This inverter was connected to the grid through a simple L-filter. Regulated DC power supply was used as the input voltage. Table I shows the parameters used for the simulation and the experimental setup.

The PSIM software was used for our simulation analysis. Figure 10 shows the first simulation results of the study of the boost capability along with DC-link utilization. Similar to Figure 8, it shows the hysteresis band and the DC-link voltage dependences versus the input power. The main goal was to define a minimum DC-link voltage with a sinusoidal injected to the grid current. An open-loop control system with manual tuning $\Delta S$ was used.

Figure 10(a) illustrates the dependence of the DC-link voltage $V_{DC}$ versus the input voltage $V_{IN}$, while Figure 10(b) shows the dependence of the auxiliary band ratio $\Delta S$ versus the input voltage $V_{IN}$. Total hysteresis band was equal to 2 A. Reference root mean square (RMS) output current was about 5 A for all simulated points.

The results obtained are close to those theoretically predicted in Figure 8. At the same time, it can be seen that in the low-input voltage area, the DC-link voltage is slightly higher than that theoretically expected. If (or when) the input voltage rises, the DC-link voltage tends to that theoretically expected. It should be noted that simulation model was adjusted in accordance with the experimental prototype, taking into account all parasitic parameters.

The main reason of difference in the theoretical and simulation results lies in finite passive component values. Because of single-phase power fluctuation, capacitor oscillations in the ZS and qZS inverter.

![Figure 9. Single-phase ZS/qZS inverter.](image)

Table I. System parameters used for simulation and experiments.

<table>
<thead>
<tr>
<th>System parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input DC voltage $V_{IN}$</td>
<td>40–360 V</td>
</tr>
<tr>
<td>Output AC RMS voltage $V_{M}$</td>
<td>230 V</td>
</tr>
<tr>
<td>Capacitance value of the capacitors $C_1$, $C_2$</td>
<td>2 mF</td>
</tr>
<tr>
<td>Inductance value of the inductors $L_1$, $L_2$</td>
<td>580 $\mu$H</td>
</tr>
<tr>
<td>Inductance of the filter inductor $L_f$</td>
<td>2.2 mH</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>250 kHz</td>
</tr>
</tbody>
</table>
qZS networks lead to the DC-link fluctuation. As a result, the minimum level can be significantly lower, and the sinusoidal shape of the injected current is not achieved despite the high average DC-link level. At the same time, this phenomenon is insignificant at higher input voltages where high voltage boost is not required.

At the same time, Figure 10 reveals the difference between the ZS and qZS networks. It can be seen that in the qZS network $V_{DC}$, the voltage and $\Delta S$ are higher than in the ZS network. The reason is that the qZS network is sensitive to the current conduction mode. In the DCM, the desired instantaneous DC-link voltage level can be lower, and therefore, it requires additional increase in the auxiliary band ratio $\Delta S$, which in turn, causes additional rise in the peak DC-link voltage.

Figures 11 and 12 show a set of simulation diagrams in the steady-state mode for the qZS network. Figure 11 illustrates the simulation results for the 240 V input voltage and simple hysteresis control. Figure 11(a) and (b) shows the grid current along with the voltage and the DC-link voltage along with the input voltage over one fundamental period, respectively. Figure 11(c) illustrates several switching cycles of the DC-link voltage along with the output current.

Despite lower input voltage, the DC-link voltage level is sufficient to inject current to the grid. Switching frequency ranges from 5 to 25 kHz. It should be mentioned that low switching frequency matches the zone with the largest amplitude of the grid current.

Figure 12 corresponds to the same input voltage but with modified hysteresis control. Total hysteresis band was equal to 2 A in both cases, and the auxiliary shoot-through hysteresis band was equal to 0.8 A ($\Delta S = 0.4$). RMS output current was about 5 A. It means that by controlling that value,
we can control the necessary boost capability of the inverter. That parameter and the value of the grid-connected inductance $L_g$ strictly define the switching frequency range and the THDI of the injected current. It can be noted that minor changes in the THDI of the injected current and switching frequency are within hysteresis modifications. In the studied point, the THD decreased from 9% to 7%, maximum switching frequency increased from 25 to 40 kHz.

Finally, to prove our theoretical and simulation predictions, a simple low-voltage low-power qZS-based DC–AC experimental prototype was assembled. Passive element values corresponded to those used in the simulation. Figure 13 shows the experimental waveforms in the steady-state mode in accordance with the simulation results. A modified 2L hysteresis control method was used. The control board was based on the low cost FPGA. Fast external AD-converters enable high sampling frequency (250 kHz) to be achieved.

The grid current and the grid voltage are depicted in Figure 13(a). The RMS value of the grid voltage was about 58 V, and the current was 2.5 A, and the injected power was about 150 W.

The DC-link voltage and the input voltage are shown in Figure 13(b). It confirms the presence of shoot-through states along with the DC-link boost. At the same time, Figure 13(c) illustrates the hysteresis shoot-through algorithm. Several shoot-through states, when the DC voltage is equal to

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zero, are applied when current flows through the auxiliary shoot-through hysteresis band. Input voltage was equal to 70 V, DC-link amplitude voltage reached 110 V. Maximum total hysteresis band was set to 0.5 A, while the maximum auxiliary shoot-through hysteresis band was 0.2 (0.1 A – absolute value).

It should be noted that in this simple case, the switching frequency was in a range from almost zero to 10 kHz, while the measurement sample frequency was 250 kHz.

5. CONCLUSIONS

This paper presents a novel hysteresis current control technique with the distribution of shoot-through states. The operation principle of the novel algorithm is provided by a detailed description and the steady-state analysis.

The steady-state analysis for the ZS/qZS network showed that such approach provides a wide input voltage gain regulation capability along with maximum DC-link utilization. Several possible modifications presented are intended for current quality improvement and extension for three-level and multi-level inverter applications.

Simulation and experimental results confirmed our theoretical hypothesis. Slight deviations from the results theoretically expected are explained by the assumptions that were accepted within analysis.

This control algorithm could be applied in any buck-boost single-stage inverter topology with IS network where shoot-through states are required. Because of the features presented previously, it is well suited for any renewable energy grid-connected applications.

Hysteresis current control based closed-loop system for grid-connected applications can be easily realized by means of a low cost FPGA or a microcontroller. Also, such advanced control functions as active filtering can be easily implemented in such control strategy.

For practical reasons, switching frequency range must be limited during the design in order to avoid possible resonance problems in the IS network and the output filter. In the case of IS networks (qZS) with continuous input current, attention should be carefully paid to passive element design in order to avoid the DCM. This phenomenon and general DC-link voltage fluctuations in any IS network require deeper analysis.

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