Identification of spatial localization and energetic position of electrically active defects in amorphous high-κ dielectrics for advanced devices

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Abstract

In this work, we report the use of the conductance transient technique (GTT) to evaluate disordered-induced gap states (DIGS) in gate dielectrics of metal-insulator–semiconductor (MIS) structures. These states are electrically active defects inside the dielectric bulk which are preferentially located at regions near the dielectric/semiconductor interface. Conductance transients occur when the MIS structure is driven from deep to weak inversion, at various frequencies and temperatures, allowing us to obtain contour line maps of defects spatially and energetically distributed inside the dielectric. This method has been applied to evaluate DIGS densities in advanced high-κ gate dielectrics, such as HfO₂, Al₂O₃, TiO₂, silicates and other mixtures grown on silicon substrates by atomic layer deposition under different process conditions. Commonly, high DIGS densities involve low interface state densities Dି and vice versa, indicating that there is some kind of interaction or evolution between these two types of defects or traps. An explanation for the dynamics dictating the transformation of interface states to DIGS states is a key point in determining the quality of the dielectric films.

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1. Introduction

Recently, great effort has been devoted to the development of high-κ dielectrics which can replace SiO₂ thermally or chemically grown as the gate insulator of metal-oxide–semiconductor field-effect-transistors [1]. Epitaxial dielectrics are complicated to grow, though, and amorphous dielectrics may be preferred in order to minimize surface roughness and field variations experienced by electrons traveling in the channel adjacent to the gate dielectric, leading to excess scattering and channel mobility degradation. However, defects existing in these emerging materials play an important role in device operation, so their use in micro- and nano-semiconductor technology can be seriously endangered. Unfortunately, the nature and formation of these defects is not well known, so the study of the defects is a primary concern to be able to apply techniques which can minimize them. Since electrically active defects are atomic configurations which give rise to electronic states in the band gap, developing an atomic-scale understanding of defects is mandatory.

Several methods have been developed to obtain defect densities at insulator/semiconductor interface [2], such as
deep level transient technique (DLTS), high and low (quasi-static) frequency capacitance–voltage measurements, etc. However, the study of defects existing inside the gate dielectric bulk is not so widely established. In this work, we show how the conductance transient technique (GTT), developed by us, is very useful when exploring defects not only at insulator/semiconductor interface but also distributed inside the dielectric. This technique has been applied to several amorphous thin high-k dielectric films atomic layer deposited (ALD) on silicon under different conditions. From transient conductance measurements we have obtained contour maps showing the spatial and energetic distribution of electrically active defects inside the dielectric, preferentially located at regions close to the dielectric/semiconductor interface. A comparative analysis of these maps provides valuable information about the influence of technological deposition conditions, as well as materials on defect distribution. The materials studied were binary oxides, namely HfO$_2$, TiO$_2$, Al$_2$O$_3$, Ta$_2$O$_5$, and mixtures: HfSi$_x$O$_{1-x}$, Zr–Al–O, Hf–Al–O, Zr–Al–Nb–O, Hf–Al–Nb–O [3].

2. Conductance transient technique (GTT)

We have previously shown [4] the existence of conductance transients in MIS structures which are driven from deep to weak inversion. This behavior is explained in terms of disorder-induced gap states (DIGS) continuum model suggested by Hasegawa et al. [5]. These authors proposed that lattice breaking at semiconductor/insulator interface causes defects with a continuous distribution both in energy and in space. Conductance transient phenomena are due to charge and discharge of DIGS states assisted by majority carriers coming from the corresponding semiconductor band by means of a tunneling assisted mechanism. Transients can be understood looking at Fig. 1 which is referred to a MIS structure over an n-type semiconductor substrate. When the bias pulse is applied, empty DIGS trap electrons coming from the conduction band (n-MIS structure). $E_F$ and $E'_F$ are the locations of the Fermi level before and after the pulse. Capture process is assisted by tunneling and is, thus, time consuming, so empty states near the interface capture electrons before the states deep in the dielectric. $x_C$ is the distance covered by the front of tunneling electrons during the time $t$. It is important to note here that only those states with emission and capture rates of the same order of magnitude than the frequency have non-zero contributions to the conductance [6]. If an experimental frequency $\omega$ is assumed, only those states with emission rates in the range $\omega \pm \Delta \omega$ can contribute to the conductance (those located over equiemission line $\epsilon_p = \epsilon_0$), so only when the front of tunneling electrons reaches point A conductance increases. Then, when point B is reached, conductance transient follows the DIGS states distribution which is typically decreasing as we move away from interface, in agreement with Hasegawa’s model [5]. Finally, conductance returns to its initial value when the front reaches point C, since after this point DIGS states susceptible to contribute to the conductance signal have energies strongly apart of the Fermi level and, then, they remain empty.

In the following, we show the model developed by us [7] to obtain DIGS states as a function of the spatial distance to the interface and the energy position by measuring conductance transients at different frequencies and temperatures. The calculation details presented here are for the case of an n-MIS structure. Similar equations can be derived for p-MIS devices. Our model departs from the conductance method typically used to obtain the interface state density, $D_{it}$, in MIS devices. For an angular frequency, $\omega$, $D_{it}$ is related to conductance by the equation $D_{it} = \frac{G_{ss}}{\omega C_0}$, where $G_{ss}$ is the stationary value of the conductance. Variations of this value are due to the DIGS contribution to the conductance:

$$N_{DIGS} = \frac{(G(t) - G_{ss})}{0.4qA\omega} = \frac{\Delta G(t)}{0.4qA\omega}. \quad (1)$$

The distance covered by the front of tunneling electrons during the time $t$, $x_C(t)$, is given by [5]

$$x_C(t) = x_{on} \ln(\sigma_0 v_{th} n_i t), \quad (2)$$

where $x_{on} = \frac{h}{\sqrt{4m_0\varepsilon_0 H_{eff}}}$ is the tunneling decay length, $\sigma_0$ is the carrier capture cross-section value for $x = 0$, $v_{th}$ is the carrier thermal velocity in the semiconductor, and $n_i$ is the free carrier density at the interface. Finally, $m_{eff}$ is the electron effective mass at the dielectric and $H_{eff}$ is the insulator–semiconductor energy barrier for majority carriers, that is, the dielectric to semiconductor conduction band offset. One can see that $x_{on}$ is higher for dielectrics in which $H_{eff}$ and $m_{eff}$ are low. In these cases, the tunneling front $x_C$ is faster and, consequently, transients reach deeper locations in the dielectric. Fig. 2 shows $x_{on}$ for some high-k dielectrics (electron effective mass and barrier height values have been obtained from Refs. [9] and [1], respectively). An important trend can be derived from this figure: as permissivity increases, tunneling decay length increases providing deeper DIGS profiles.

Finally, to obtain the energy position of DIGS states in the band gap of the dielectric, we use equiemission line.
equations [10], and considering that the measurement frequency is related to emission rate by \( e_n = \omega / 1.98 \) [6], we obtain the next equation:

\[
E_{CSC} - E_T = kT \ln \left( \frac{\sigma_0 e_n N_C}{\omega / 1.98} \right) - kT x_{on} x_C(t). \tag{3}
\]

When temperature decreases the emission rates of all interface states exponentially decrease, and the equilibrium lines shift approaching the interface. Thus, transients are modified in a similar way as when frequency is increased while keeping constant the temperature. DIGS three-dimensional profile or contour line maps can be obtained using Eqs. (1)–(3).

As for the experimental precision, temperature measurement involves an error of ±0.1 K. Estimated errors of energy and defect concentration values on DIGS profiles are of about ±10 meV and \( 5 \times 10^{-9} \text{ eV}^{-1} \text{ cm}^{-2} \), respectively. Estimated precision on DIGS depth is of about 2 Å.

3. Experimental DIGS contour maps for high-\( k \) dielectrics

The experimental set-up consists of the HP 33120A arbitrary waveform generator to apply the bias pulses and the EG&G 5206 lock-in analyzer to measure the conductance. An HP 54501A digitizing oscilloscope records conductance transients. Samples were cooled in darkness from room temperature to 77 K in an Oxford DN1710 cryostat. An Oxford ITC 502 controller was used to keep constant the temperature during measurements.

In this section we review results obtained for several high-\( k \) dielectrics grown by atomic layer deposition (ALD) under different processing conditions. The most noticeable results provided by the experimental contour maps are outlined.

3.1. Hafnium-based dielectrics

HfO\(_2\) is a promising gate dielectric material due to its high dielectric constant and excellent thermal stability. Fig. 3 shows three-dimensional DIGS plots for HfO\(_2\) atomic layer deposited on n-Si (Fig. 3(a)) and over p-Si (Fig. 3(b)) using chloride as the metal precursor. DIGS states are located at energies close to the majority band edge of the semiconductor. This can be explained in terms of the very nature of the conductance transient technique: majority band edges have the maximum majority carrier concentration, so states located at energies close to this position have the maximum probability to capture majority carriers. On the other hand, no conductance transients were observed for samples thinner than 40 Å. Kerber et al. [11] proposed the existence of a defect band in the HfO\(_2\) layer. We find spatially distributed defect bands for films on both types of silicon substrates. These defects bands could be due to oxygen vacancies: when the capacitor structure is terminated by the oxide–Si interface, the electric field existing in the dielectric film moves. For instance, oxygen vacancies (positively charged) are located farther away from the interface in samples deposited on n-type silicon because of the difference in semiconductor band bending at the interface [12].

We obtained maximum interfacial state density values of about \( 5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1} \) for p-type substrate, and \( 4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1} \) for n-type substrate [12]. Autran et al. [13] measured maximum interfacial state density values of \( 13.2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1} \) in n-type MOS capacitors with a
gate dielectric stack of 7.7 nm HfO2 oxide deposited by atomic layer chemical vapor deposition (ALCVD) on a 0.7 nm native Si oxide film. This high value can be related to the partial transformation of the initially stoichiometric SiO2 into a hafnium silicate HfSiO3 layer after gate deposition, as it has been demonstrated by these authors. Indeed, high values of interfacial state density (near to $1 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$) have been measured in hafnium-rich silicate-based MOS structures [14].

Forming gas annealings (FGA) are usually employed in integrated circuit technology for passivation of defects (dangling bonds) on Si surface. Fig. 4 shows DIGS density corresponding to post-metallization annealed (400 °C, 30 min) Al/HfO2/p-Si sample. Lower DIGS density is achieved, but $D_{it}$ density is increased in this sample [15], indicating that thermal treatment partially moves the insulator defects to the interface. Ioannou-Sougleridis et al. [16] attributed instabilities observed in as-grown Y2O3 samples to slow traps, which were mostly removed after FGA. The same behavior can affect our results.

Transition metal silicates, such as hafnium silicate, have also been the object of a considerable number of studies to replace SiO2 because of their higher crystallization temperature. Fig. 5 shows DIGS states obtained from as-deposited Al/HfSiO3/n-Si structures grown using HfI4 and Si(O2C2H5)4 as precursors. In this case contour lines have a more anisotropic shape than those for HfO2 indicating less homogeneous distribution of DIGS defects. In fact, we can see two different local ordering at zones A and B. The boundary between these zones approximately follows the line $E_{Csc} - E_T = 588.22 - 15.42X_C$. Contour lines are parallel in zone A and perpendicular to this boundary, indicating some regularity in the defect distribution. On the other hand, DIGS density rapidly decreases to lower values in zone B, where uniformity is higher. When this sample is submitted to a post-deposition annealing at temperatures ranging from 700 to 800 °C, this behavior of two different zones is unchanged [17].

3.2. Al2O3

The importance of Al2O3 as an insulating dielectric is due to its large band gap (8.8 eV), excellent stability when deposited over silicon and its amorphicity – Al2O3 is a good glass former. We have studied Al/Al2O3/n-Si structures grown by atomic layer deposition at temperatures ranging from 300 to 800 °C. AlCl3 and H2O were used as precursors.

DIGS states densities are listed in Table 1. The measured value is similar in all samples, but unmeasurable at 500 °C. It is possible that Al2O3 grown at this temperature is free of residual defects and moreover, the amorphicity, high purity and structural homogeneity achieved cause low defect densities, making the conductivity signal difficult to measure. In Fig. 6 one can see the contour plot corresponding to the sample grown at 300 °C. The shape is similar to HfO2 sample deposited on n-Si, but in the case of Al2O3 the maximum density appears near the interface which might cause quicker discharging of the defects.

The highest quality sample in terms of DIGS states is that grown at 500 °C, but if we consider also interface states densities obtained for these samples [18] the best sample would be that grown at 300 °C. It is important to consider both $D_{it}$ and DIGS densities before concluding the quality of the samples.

3.3. TiO2

TiO2 is being extensively studied for memory and logic applications, because of its high dielectric constant, ranging from 40 to 86. We have studied TiO2 atomic layer deposited on etched n-silicon and high-pressure reactive sputtered over SiO2-covered Si. DIGS state densities and other growth parameters are listed in Table 2. All ALD samples have been annealed at 750 °C, so the only differences are growth temperature and chemical precursors. H2O seems to be more adequate as a precursor than H2O2 for both temperatures. On the other hand, when TiCl4 is used as precursor, chlorine remains in the film whereas when Ti(O2C2H5)4 is used, carbon remains in the films. Carbon has been found uniformly in the film bulk.
but it is known that chlorine accumulates near the interface [20]. Because of that, higher DIGS and lower DIGS values are seen in the films grown with TiCl₄ and H₂O. TiO₂/SiO₂ dielectric thin films stacks were grown on n-type silicon substrates. A 7 nm layer of SiO₂ was deposited by an electron cyclotron resonance (ECR) oxygen plasma oxidation. Afterwards, 77.5 nm TiO₂ films were grown in an HPRS system at a pressure of 1 mbar during 3 h and at a temperature of 200 °C. Finally, some samples were in situ annealed in oxygen atmosphere at temperatures ranging from 600 to 900 °C. Sputtered films exhibit lower DIGS densities, but the large band gap buffer layer (SiO₂), interposed between substrate and TiO₂ inhibits trap displacements from the interface to the dielectric bulk.

**Table 1**

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Maximum DIGS (x10^{11} cm⁻² eV⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T₁ = 300 °C</td>
<td>12</td>
</tr>
<tr>
<td>T₂ = 400 °C</td>
<td>19</td>
</tr>
<tr>
<td>T₃ = 500 °C</td>
<td>Undetectable</td>
</tr>
<tr>
<td>T₄ = 600 °C</td>
<td>15</td>
</tr>
<tr>
<td>T₅ = 800 °C</td>
<td>25</td>
</tr>
</tbody>
</table>

Fig. 6. Contour plot of DIGS density obtained to Al/Al₂O₃/n-Si (oxide grown at 300 °C).

**Table 2**

<table>
<thead>
<tr>
<th>Precursors</th>
<th>TiO₂ atomic layer deposited over n-Si</th>
<th>TiO₂ sputtered over SiO₂</th>
</tr>
</thead>
<tbody>
<tr>
<td>T₁ (°C)</td>
<td>Maximum DIGS (x10^{11} cm⁻² eV⁻¹)</td>
<td>Maximum DIGS (x10^{11} cm⁻² eV⁻¹)</td>
</tr>
<tr>
<td>Ti(OC₂H₅), H₂O</td>
<td>275 0.1</td>
<td>No</td>
</tr>
<tr>
<td>Ti(OC₂H₅), H₂O</td>
<td>225 3.5</td>
<td>600 0.5</td>
</tr>
<tr>
<td>Ti(OC₂H₅), H₂O</td>
<td>275 1</td>
<td>700 2.6</td>
</tr>
<tr>
<td>TiCl₄, H₂O</td>
<td>225 2</td>
<td>800 1.2</td>
</tr>
<tr>
<td>TiCl₄, H₂O</td>
<td>225 2</td>
<td>900 Not detected</td>
</tr>
</tbody>
</table>

**Fig. 7.** Contour plots of DIGS density obtained to ALD TiO₂ sample grown at 225 °C from TiCl₄ on etched silicon (a) and TiO₂ sputtered on SiO₂-covered silicon (600 °C annealed) (b).

3.4. Other materials: mixtures

Mixtures, ternary or quaternary oxides are also studied in order to find replacement for SiO₂. Aluminium is a good glass former, so it can amorphize other dielectric layers. But this would decrease permittivity. To avoid this fact, niobium is also mixed with dielectrics, due to its high permittivity. We have studied Hf–Al–O, Zr–Al–O, Hf–Al–Nb–O and Zr–Al–Nb–O mixtures. Ta₂O₅ layers have also been compared to Ta–Nb–O mixture. All these materials can be atomic layer deposited on p-silicon, using chlorides as Hf and Zr precursors, Al(CH₃)₃ as Al precursor, and ethoxides as Nb and Ta precursors. Table 3 shows DIGS densities of these dielectric layers. In all cases niobium possibly acts as a barrier which inhibits trap displacement from the interface: in fact interface state densities are larger when Nb is incorporated and at the same time, DIGS state densities are reduced [21,22]. Hf–Al–O and Zr–Al–O behave very similarly due to the similarity between hafnium and zirconium. DIGS density for Ta₂O₅ has an
The best trade-off is obtained for samples grown at 300 °C. Interface states densities obtained for these samples are mixed with niobium, DIGS densities decrease indicating that niobium inhibits trap displacement from the interface. The most important conclusion of all our observations is that both interface states and DIGS must be taken into account when qualifying a high-k gate dielectric.

**Acknowledgements**

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**References**


**Table 3**

<table>
<thead>
<tr>
<th>Mixture</th>
<th>Maximum DIGS (cm⁻² eV⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HF–Al–O</td>
<td>1.2 × 10¹²</td>
</tr>
<tr>
<td>HF–Nb–Al–O</td>
<td>2 × 10⁸</td>
</tr>
<tr>
<td>Zr–Al–O</td>
<td>2 × 10¹²</td>
</tr>
<tr>
<td>Zr–Nb–Al–O</td>
<td>Not detected</td>
</tr>
<tr>
<td>Ta₂O₅</td>
<td>1.2 × 10¹¹</td>
</tr>
<tr>
<td>Ta–Nb–O</td>
<td>Not detected</td>
</tr>
</tbody>
</table>

**Fig. 8.** Contour plot of DIGS density obtained to Al/Ta₂O₅/p-Si (oxide grown at 300 °C).