An XML-based Test Development and Deployment Framework for Mixed-Signal and Digital Devices

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INTRODUCTION

In integrating IP into SoC-s, it is essential to provide the IP configuration, integration data (SPIRIT, IEEE P1685), and the test vectors and timing with the core design (CTL, IEEE 1450.6). When complemented by actual configuration data for the ATE hardware, it radically shortens the time required for local and customer test runs.

MOTIVATION

This work extends the concepts presented at the IOST'07 Workshop (VTS'07).

-- **Increase automation in test processes**;

-- **Seek correlation among various phases**;

-- **Analyze correlation data**;

-- **Optimize assigned resources, timing, etc**.

-- **"EDA-aware ATE"** and **"ATE-aware EDA"**

-- **Sequentally generate XML schemas.**

STANDARDS

-- **CTL** (Core Test Language,IEEE P1450.6)

-- **STIX** (Semiconductor Test Interface eXtensions)
- an evolving initiative on tester-wafer connections.

XML-based standards:

-- **ATML** (Automatic Test Markup Language,IEEE P1671)
- test, DUT, equipment, results, conf. descriptions.

-- **IP-XACT**(Core Test Language,IEEE P1685)

FRAMEWORK

Tools employed:

-- **Synopsys** coreAssembler

-- **Mentor** PlatformExpress

-- **TurboTester** (ATPG)

-- **APRICOT** (verification, ATPG, *CTL output*)

-- **XML::LibXML** Perl module (XML processing)

-- **eXist** / **XML::DB** (test data storage)

-- **LabVIEW** (User Interface, XML visualization)

The above are free software or widely available to the academia and the industry. A project website is developed to enhance the co-operation.

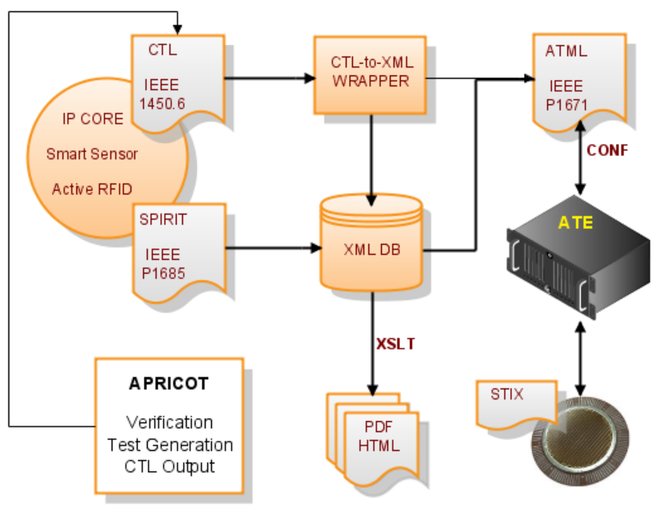

Figure 1. Framework outline

METHODOLOGY

CTL-to-XML concept is analyzed (*Ref: Table 1*) and prototyped for a subset of elements, extended upon requirements. **CTL/STIL output capability for APRICOT** was developed. XSLT enables visual and multiple format support .Fast generation of human-readable reports and data-sheets with performance figures is enabled.

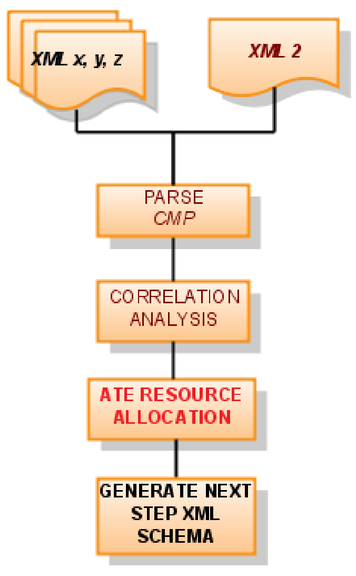

Figure 2. XML processing flow

It acts as middle-ware between data sheet repository and internal design-and-test, layers of confirmation and information sign-off in between.

Utilizing XML for the STIL formats has been discussed in the STIL WG - no decision yet whether to actually adopt XML as the underlying format.

+ Data robustness, human-readability;
+ Wide format acceptance;
+ Availability of parsing tools.

- Description overhead;
- Additional development efforts.

STIL AMS is being reviewed, addressing mixed-signal test. Appropriate additions were proposed to the ***Signal Block*** and ***TesterChannelMap*** syntaxes. A new block, ***AMS Block,*** was proposed. CTL and STIL AMS are hierarchically structured formats - parsing and mapping to XML is an integration task. The sample *SetList* and proposed XML equivalent are given in Table I.

TABLE I
STIL AMS -TO- XML MAPPER (AMS_SETLIST SAMPLE)

STIL AMS	XML Proposal
AMS_SetList {	<AMS_SetList>
AMS_Set test1 {	<AMS_Set>test1</AMS_Set>
ActiveConnection toto; Signal VPLUS {	<ActiveConnection>toto</ActiveConnection> <Signal>VPLUS</Signal>
Resource DC {	<Resource>DC</Resource>
Force_V = '10V'; Clamp_I = '200mA'; Measure = Strobe_I; Range_I = '20mA'; Guards = ON; SlewRate = '400.0e03V/s'; }	<Force_V>10V</Force_V> <Clamp_I>200mA</Clamp_I> <Measure>Strobe_I</Measure> <Range_I>20mA</Range_I> <Guards>ON</Guards> <SlewRate>400.0e03V/s</SlewRate>
}	</AMS_SetList>
}	
}	

CONCLUSIONS

Strong acceptance of and move to open source tools, open standards and interoperability is a driving force behind several industry-led initiatives, thus also enabling deeper co-operation with the academia. Several universities (incl. TUT) are members of the Semiconductor Test Consortium.

FUTURE WORK

Test objects include a **mixed-signal controller core**, **PMU**s, **sensors** and **RFID**-based devices. LabVIEW is evaluated as an option for GUI.

REFERENCES

[1]STIL-AMS notes from ITC, http://grouper.ieee.org/groups/1450/dot-ams/VTS-2005.pdf

[2]STIL Working Group meeting minutes, http://grouper.ieee.org/groups/1450/dot1/0040_min.txt , March 2008

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AUTHOR BIO

Andres Mellik (S'07) obtained a B.Sc. and M.Sc in EE (Measurements) from TUT respectively in 2002 and 2005. In 2004, he obtained a M.Eng. in Embedded Systems Design from AlaRI, Univ. of Lugano, Switzerland. He is obtaining a PhD in EE from TUT on automated test generation for mixed-signal circuits and devices. Research interests include automated test standards and development of, embedded systems and DSP performance testing issues.