Study of surface defects in 4H-SiC Schottky diodes using a scanning Kelvin probe

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Abstract. In the present paper we attempt to study and explain the increased leakage currents in Schottky diodes with an integrated p-n structure. Using a scanning Kelvin probe method (vibrating capacitor) the local variations of surface contact potential difference (CPD) were obtained for chips with large and small leakage currents. It is shown that samples with higher leakage currents have a smaller surface potential barrier. The SEM investigations revealed that the dislocations penetrating from the substrate into the epitaxial layer play a critical role in increasing leakage currents.

Introduction

In our earlier work [1] the results of a statistical study of leakage currents in commercial high voltage JBS diodes were presented. The characteristics of 147 chips were measured. Measurements of leakage currents were performed at room temperature at a fixed reverse voltage of 1440 V. Despite the fact that the reverse currents did not exceed the designed values (10 µA), the variation in the currents was significant: from 10 nA to 6 µA (i.e. three orders of magnitude). Figure 1 shows the most typical reverse current-voltage characteristics of the three chips, selected from groups with different leakage currents. Considerable variation in the magnitude indicates a defective nature of the leakage currents. However, the DLTS spectra for the chips with different leakage currents were identical (all diodes present S-centers of the same concentration). The nature of the current-voltage characteristic and DLTS spectra testified that the reverse currents flow on the defects, not a point but on linear. Based on previous studies (e.g. [2, 3]) it was concluded that the dislocations penetrating the epitaxial layer are the main reason for such a large difference in leakage currents. Moreover, the revealed dislocation density in the tested chip was quite high (about $10^4$ cm$^{-2}$ on average). The goal of the work presented below is to provide an additional confirmation of this version through the use of other tools (e.g. the Kelvin probe method and SEM microscopy).
Methodology

CPW3-1700S010 diode chips (Cree) were used for the experimental studies. The diodes are designed for a direct current of 10 A, a reverse voltage of 1700 V, and reverse currents of < 10 µA at room temperature. The chips used for the investigations were selected on the principle of the large difference in reverse currents (compare chip 1 with 4300 nA and chip 3 with 15 nA @ 1440 reverse volts (Fig. 1)). After testing the I-V characteristics, the metal Schottky contacts were removed from the surfaces of the chips. The surface potential barrier measurements were performed in the dark and under illumination using the Kelvin probe Trek model 320C equipped with a 4 × 4 mm reference electrode made of glass covered by a transparent and conductive tin-oxide thin film. The measurement procedure is detailed in [4].

To identify the dislocation pattern the contact surfaces of the chips were etched in molten KOH at 500 ºC for 20 min. To investigate the specificity of the dislocation pattern a Zeiss model EVO MA-15 SEM fitted with an INCA energy system by Oxford Instruments was used.

Results and discussion

Figure 2 shows the contact potential densities on the contact surfaces of the chips in (a) equilibrium (in the dark) and (b) nonequilibrium (light excitation) states; in (c) the maps show the difference between "dark" and "light" measurements.

As follows from the methodology proposed in [4] the surface potential in the equilibrium state is:

\[
V = \frac{Qd_{ox}}{\varepsilon_{ox}} + \Psi(Q + Q_{ss}) + \Phi_{ms}.
\]  

That is, the total potential \( V \) is the sum of the voltage drop in the oxide (\( V_{ox} = Qd_{ox}/\varepsilon_{ox} \)), the voltage drop in the semiconductor (\( \Psi \), surface potential barrier determined by the charge on the oxide surface, the semiconductor-oxide interface states charge, and the charge in the depletion region of the semiconductor), and (\( \Phi_{ms} \)) is the work function difference between the reference electrode and the semiconductor. In Eq. 1, \( d_{ox} \) is the oxide thickness and \( \varepsilon_{ox} = \varepsilon\varepsilon_0 \) is the oxide permittivity.

Taking into account that the thickness of the oxide, as well as factors associated with the corresponding states, is the same for both chips, the difference in surface potential can be associated only with a difference in surface potential barrier (\( \Psi \)). In the presence of high intensity light excitation the band bending disappears (the second term in Eq. 1 also disappears). The surface potential \( V_{FB} \) can be written as:

\[
V_{FB} = \frac{Qd_{ox}}{\varepsilon_{ox}} + \Phi_{ms}.
\]  

Fig. 1. Reverse current-voltage characteristic for the three diode chips at room temperature.

Chip 1 4300 nA @ 1400 V
Chip 2 360 nA @ 1400 V
Chip 3 15 nA @ 1400 V
Thus, the vibrating capacitor measurement in the dark combined with light excitation measurement gives the surface potential barrier as:

\[ \Psi = V - V_{FB}, \]

where the surface potential barrier is the difference between the “dark” and “light” values of the measured oxide surface potential. So, as seen from Fig. 2, the surface potential barrier changes in the intervals of –400 to –450 mV for chip 1 and –500 to –700 mV for chip 3.

When the above conditions are taken to be equal, the distribution of surface potential is equivalent to the distribution of potential barrier height on the active area of the diode chips.

However, the dislocation pattern revealed by etching in molten KOH paradoxically does not meet expectations. Dislocation density is higher on the surface of the chip with the lower leakage current than in the chip with the large leakage current. The dislocations on the surface of chip 1 are not
uniformly distributed but have a non-uniform density and a density in clusters of $\sim 1.4 \times 10^4 \text{ cm}^{-2}$. Dislocations in chip 3 have a uniform distribution with an average density $\sim 3.1 \times 10^4 \text{ cm}^{-2}$. Most likely the reason for this is the different type of dislocation. As seen in the larger scale picture, chip 1 has relatively large pits with an off-axis angle of 8º, which is a characteristic orientation for the 4H-SiC substrate. So, in chip 1, we have to deal with the dislocations propagating from the substrate into the epitaxial layer. The pits in chip 3 have an off-axis angle close to 0º and are shallow screw dislocations formed during epitaxial layer growth. Thus, we have reason to believe that the penetration of dislocations leads to an increase of leakage current in the tested diodes.

**Summary and conclusions**

Up to date the effect of dislocations on the current-voltage characteristics of SiC Schottky diodes has been the subject of dozens of works. However, all the works are of fragmented nature, and this will continue until a good physical model of the effect of dislocations on I-V characteristics is built. We also tried to contribute to this problem using the Kelvin probe method in order to link the surface potential with the distribution of dislocations on the surface of the diode chip. It must be stated that the resolution of this method available to date cannot reliably determine this relationship. Nevertheless, in the region of location of threading dislocations this relationship is quite clearly visible (e.g. chip 1; compare Fig. 2 and Fig. 3). Thus, there is every reason to continue this work.

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