Interlock Delay Time and its Influence on the Operability and Efficiency of High-Power DC/DC Converters

Abstract. In DC/DC power converters the interlock delay time between IGBT switching on and off in the opposite inverter arms is usually recommended to be 10-20% of the half period to avoid a short circuit in a DC-link. However, in power supplies with extended input voltage variations, much smaller interlock delay time could be used. In this paper the interlock delay time minimization possibility is analyzed on an example of an experimental DC/DC converter with 6.5 kV IGBTs. The possible impact on the converter’s components, operability and efficiency are evaluated.

Streszczenie. W celu uniknięcia zwarcia obwodu DC w przekształtnikach DC/DC stosuje się zwykle czas martwy równy 10-20% połowy okresu pracy. W przypadku dużej zmienności napięcia wejściowego wymagane są znacznie krótsze cześci martwe. W artykule przedstawiono analizę minimalizacji czasu martwego oraz wyniki laboratoryjne z przekształtnikiem DC/DC z tranzystorami IGBT 6.5 kV. Zbadano możliwy wpływ minimalizacji czasów martwych na podzespoły przekształtnika, możliwość jego pracy i sprawność. (Czas martwy i jego wpływ na funkcjonalność i sprawność przekształtników DC/DC dużej mocy)

Keywords: DC/DC power conversion, interlock delay time, IGBT, pulse width modulated power converters.
Słowa kluczowe: przekształtniki DC/DC, czas martwy, IGBT, przekształtniki z modulacją impulsową.

Introduction

Selection of a proper interlock delay time for a voltage source inverter with IGBTs is one of the first steps an engineer must take when starting to design a switch mode power converter. Too long interlock delay time may lead to higher filtering inductances and increased semiconductor losses. Too small interlock delay can cause the shoot trough of inverter bridge arms, input voltage distortion, shortened lifespan of transistors, and even a failure of semiconductor switching devices.

Theoretically, the minimum interlock delay time between switching different inverter arm transistors on and off is the maximum control signal propagation delay from the control system to the IGBT plus time that an IGBT needs to turn on or off. There are many papers devoted to the interlock delay time analysis in AC/AC and DC/AC converters that produce modulated multiphase output [1], [2], but the problems related to the selection of a proper interlock delay time in transformer isolated DC/DC converters with non-modulated inverter output voltage are a topic of much less coverage. Several power electronics handbooks [3], [4] propose a 10-20% interlock delay time of half period but in most cases this number could be further minimized to provide some additional benefits.

This paper studies an interlock delay time minimization possibility in the half-brige isolated DC/DC converter (Fig. 1) with high-voltage (HV) IGBTs.

The various delay times were evaluated on the simulation models that are based on the data of the experimental setup [5] with FZ200R65KF1 transistors (Infineon) and 1SD210F2 HV IGBT driver circuits (CT-concept). The control of HV IGBTs is performed by the microcontroller XC167 from Phytec. PWM signals from the control system are transferred to the high-voltage IGBT drivers via optical fibers to provide the demanded isolation barrier (12 kV).

Technical specifications of the experimental setup are presented in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Long-term minimal input voltage</td>
<td>2.2</td>
</tr>
<tr>
<td>Long-term maximal input voltage</td>
<td>4.0</td>
</tr>
<tr>
<td>Nominal input voltage</td>
<td>3.1</td>
</tr>
<tr>
<td>Desired output power</td>
<td>50</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>1 kHz</td>
</tr>
<tr>
<td>Converter output voltage</td>
<td>0.35</td>
</tr>
</tbody>
</table>

Driving of IGBT transistors in the half-bridge configuration is very simple. The duty ratio of inverter switches is controlled in accordance with the input voltage (Fig. 2). The most challenging operation point of the converter is at the minimum input voltage, when the switch on-state time becomes maximal. Here, the threat related to the cross conduction of top and bottom arm transistors should be considered.

Fig. 1. Power circuit layout of the experimental setup

Fig. 2. Timing diagrams of a half-bridge inverter
Evaluation of minimum interlock delay time

Simultaneous conduction of top and bottom switches in the half-bridge (as well as full-bridge) configuration causes a short circuit in the primary part of the converter, commonly resulting in harmful effects. However, the operation point corresponding to the minimal input voltage, where the pulse width reaches its maximum, is always a starting point for the calculations of an isolation transformer, the selection of power semiconductors and filtering.

The right interlock delay time \( t_{IDT} \) in (2) we must know the signal propagation delay from the control system to the IGBT, including the turn-on delay, turn-off delay, rise and fall times of the transistor implemented. Every logic element, gate driver, optical transmitter and receiver has the signal propagation delay time and the output transition time. In Fig. 3 the real signal flow from the microprocessor to the transistor is shown (corresponds to the described experimental setup).

\[ t_{IDT} = (t_{PD-CS,max} - t_{on,min}) + (t_{PD-CS,min} - t_{PD-D,min}) + (t_{PD-D,max} - t_{PD-D,min}) \]

where \( t_{off,max} \) is the maximal turn-off delay time of the driver, \( t_{on,min} \) is the minimal turn-on delay time of the driver, \( t_{PD-D,max} \) is the maximal propagation delay of the driver, \( t_{PD-D,min} \) is the minimal propagation delay of the driver, \( t_{PD-CS,min} \) is the minimal propagation delay of the control system, \( t_{PD-CS,max} \) is the minimal propagation delay of the control system. The result is multiplied with the safety margin \( b \) (in this application it is 1.5).

Equation (1) uses values presented in the component datasheets. In general, the dynamic behavior of an IGBT depends on such parameters as stray inductance and parasitic capacitance of the module as well as on the resistance of the gating circuit. The switch-on \( t_{on} \) and switch-off \( t_{off} \) times of an IGBT (Fig. 4) impose their own limits during the selection of the minimum delay time value. Because of their structures, the high-voltage IGBTs are relatively slow in operation and here all the values of the turn-on and the turn-off processes should be considered:

\[ t_{on,min} = t_{on,min} + t_{f,min} \]

\[ t_{off,max} = t_{off,max} + t_{f,max} \]

\[ t_{IDT} = \frac{t_{PD-CS,max} - t_{PD-D,min}}{b} + \frac{t_{PD-CS,min} - t_{PD-D,min}}{b} + \frac{t_{PD-D,max} - t_{PD-D,min}}{b} \]

The following equation can be used to calculate the interlock delay time [6]:

\[ t_{IDT} = (t_{PD-CS,max} - t_{PD-D,min}) + b \]

where \( t_{off,max} \) is the maximal turn-off delay time of the transistor, \( t_{on,min} \) is the minimal turn-on delay time of the transistor, \( t_{PD-D,max} \) is the maximal propagation delay of the driver, \( t_{PD-D,min} \) is the minimal propagation delay of the driver, \( t_{PD-CS,max} \) is the maximal propagation delay of the control system, \( t_{PD-CS,min} \) is the minimal propagation delay of the control system. The result is multiplied with the safety margin \( b \) (in this application it is 1.5).

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\[ t_{off,max} = t_{off,max} + t_{f,max} \]

\[ t_{on,min} = t_{on,min} + t_{f,min} \]

where \( t_{PD-CS,max} \) is the maximal propagation delay of the control system, \( t_{on,min} \) is the maximal turn-on delay of the transistor, \( t_{off,max} \) is the maximal turn-off delay of the transistor, \( t_{PD-D,min} \) is the minimal turn-on delay of the transistor, \( t_{PD-D,max} \) is the minimal turn-off delay time of the transistor, \( t_{PD-CS,min} \) is the minimal turn-on delay time of the transistor, \( t_{PD-CS,max} \) is the minimal turn-off delay time of the transistor, \( t_{PD-D,min} \) is the minimal rise time of the transistor, \( t_{PD-D,max} \) is the minimal rise time of the transistor, \( t_{PD-CS,min} \) is the minimal rise time of the transistor, \( t_{PD-CS,max} \) is the minimal rise time of the transistor, \( t_{IDT} \) in (2) we must know the signal propagation delay from the control system to the IGBT, including the turn-on delay, turn-off delay, rise and fall times of the transistor implemented. Every logic element, gate driver, optical transmitter and receiver has the signal propagation delay time and the output transition time. In Fig. 3 the real signal flow from the microprocessor to the transistor is shown (corresponds to the described experimental setup).

\[ \frac{t_{PD-CS,max} - t_{PD-D,min}}{b} + \frac{t_{PD-CS,min} - t_{PD-D,min}}{b} + \frac{t_{PD-D,max} - t_{PD-D,min}}{b} \]

where \( t_{PD-CS,max} \) is the maximal propagation delay of the control system, \( t_{PD-D,min} \) is the minimal propagation delay of the driver, \( t_{PD-D,max} \) is the maximal propagation delay of the driver, \( t_{PD-CS,min} \) is the minimal propagation delay of the control system, \( t_{IDT} \) in (2) we must know the signal propagation delay from the control system to the IGBT, including the turn-on delay, turn-off delay, rise and fall times of the transistor implemented. Every logic element, gate driver, optical transmitter and receiver has the signal propagation delay time and the output transition time. In Fig. 3 the real signal flow from the microprocessor to the transistor is shown (corresponds to the described experimental setup).

\[ t_{IDT} = (t_{PD-CS,max} - t_{PD-D,min}) + (t_{PD-CS,min} - t_{PD-D,min}) + (t_{PD-D,max} - t_{PD-D,min}) \]

where \( t_{off,max} \) is the maximal turn-off delay time of the transistor, \( t_{on,min} \) is the minimal turn-on delay time of the transistor, \( t_{PD-D,max} \) is the maximal propagation delay of the driver, \( t_{PD-D,min} \) is the minimal propagation delay of the driver, \( t_{PD-CS,max} \) is the maximal propagation delay of the control system, \( t_{PD-CS,min} \) is the minimal propagation delay of the control system. The result is multiplied with the safety margin \( b \) (in this application it is 1.5).

Equation (1) uses values presented in the component datasheets. In general, the dynamic behavior of an IGBT depends on such parameters as stray inductance and parasitic capacitance of the module as well as on the resistance of the gating circuit. The switch-on \( t_{on} \) and switch-off \( t_{off} \) times of an IGBT (Fig. 4) impose their own limits during the selection of the minimum delay time value. Because of their structures, the high-voltage IGBTs are relatively slow in operation and here all the values of the turn-on and the turn-off processes should be considered:

\[ t_{on,min} = t_{on,min} + t_{f,min} \]

\[ t_{off,max} = t_{off,max} + t_{f,max} \]

where \( t_{on,min} \) is the maximal turn-on delay time of the transistor, \( t_{off,max} \) is the maximal turn-off delay time of the transistor, \( t_{PD-D,min} \) is the minimal turn-on delay of the transistor, \( t_{PD-D,max} \) is the minimal turn-off delay time of the transistor, \( t_{PD-CS,min} \) is the minimal rise time of the transistor, \( t_{PD-CS,max} \) is the minimal rise time of the transistor, \( t_{IDT} \) in (2) we must know the signal propagation delay from the control system to the IGBT, including the turn-on delay, turn-off delay, rise and fall times of the transistor implemented. Every logic element, gate driver, optical transmitter and receiver has the signal propagation delay time and the output transition time. In Fig. 3 the real signal flow from the microprocessor to the transistor is shown (corresponds to the described experimental setup).

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where \( t_{off,max} \) is the maximal turn-off delay time of the transistor, \( t_{on,min} \) is the minimal turn-on delay time of the transistor, \( t_{PD-D,max} \) is the maximal propagation delay of the driver, \( t_{PD-D,min} \) is the minimal propagation delay of the driver, \( t_{PD-CS,max} \) is the maximal propagation delay of the control system, \( t_{PD-CS,min} \) is the minimal propagation delay of the control system. The result is multiplied with the safety margin \( b \) (in this application it is 1.5).

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\[ t_{on,min} = t_{on,min} + t_{f,min} \]

\[ t_{off,max} = t_{off,max} + t_{f,max} \]
the devices in the signal flow path in the experimental device are shown in Table 3.

For the hardware implemented, the interlock delay time calculated with (1) is 8.1 μs. In case the switching frequency is 1 kHz, it forms about 1.6 % of the half period. Thus, the absolute maximum switch on-state time \( t_{on,lim} \) in that case is 98.4% from the half period and the delay time \( D_{lim} \) will be

\[
D_{lim} = \frac{t_{on,lim}}{T_{sw}} = 0.984 \frac{T_{sw}}{2} = 0.492.
\]  

Table 3. Signal propagation delay and output transition times of the investigated control system

<table>
<thead>
<tr>
<th>Hex inverter – 74HC04</th>
<th>Maximum signal propagation delay ( t_{Dpd, \text{max}} )</th>
<th>0.19·10⁻⁷ s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum output transition time ( t_{Dpd, \text{out, max}} )</td>
<td>0.15·10⁻⁷ s</td>
<td></td>
</tr>
<tr>
<td>Minimum signal propagation delay ( t_{Dpd, \text{min}} )</td>
<td>0.10·10⁻⁷ s</td>
<td></td>
</tr>
<tr>
<td>Minimum output transition time ( t_{Dpd, \text{out, min}} )</td>
<td>0.07·10⁻⁷ s</td>
<td></td>
</tr>
<tr>
<td>Optical transmitter – HFBR1522</td>
<td>Maximum output transition time ( t_{DpO, \text{max}} )</td>
<td>0.8·10⁻⁷ s</td>
</tr>
<tr>
<td>Minimum output transition time ( t_{DpO, \text{min}} )</td>
<td>0.4·10⁻⁷ s</td>
<td></td>
</tr>
</tbody>
</table>

At low \( U_{in} \), if the normal \( D_{\text{max}} \) is right at the duty cycle limit, the regulator has no reserve volt-second capability and cannot respond rapidly to a sudden load increase occurring at minimal input voltage change. It may be desirable to make the “normal” \( D_{\text{max}} \) less than the absolute limit \( D_{lim} \), to provide a little headroom in this situation. We expanded the dead time to 2%, thus the maximum switch on-state time with the new approach will be 98% from the half period \( D_{lim}=0.49 \).

Although the method (1) presents a datasheet-based calculation of a minimum possible interlock delay time, it can be used by engineers to predetermine some general values of a new converter before the project is started.

Evaluation of the impact of delay time minimization on the converter

The discussed converter must operate normally within a wide input voltage range (2.2 kV DC...4.0 kV DC). To achieve proper regulation, the inverter switch duty cycle must change proportionally to the input voltage change. While the maximum switch duty cycle \( D_{\text{max}} \) should be selected upon the system requirements (mostly limited by the interlock delay time), the minimum duty cycle can be expressed as

\[
D_{\text{min}} = \frac{U_{\text{in, min}}}{U_{\text{in, max}}} D_{\text{max}}
\]

where \( U_{\text{in, min}} \) and \( U_{\text{in, max}} \) are the long-term minimum and maximum input voltages of the converter. It must be stated here that the minimization of the interlock delay time will be followed by the proportional increase of the switch duty cycle. The comparison of the converter regulation range with the old (20% from the half period) and the new minimized (2% from the half period) interlock delay time is presented in Table 4.

Table 4. Investigated change of duty cycle boundary limits

<table>
<thead>
<tr>
<th>Boundary operating points</th>
<th>Long-term minimal input voltage ( U_{\text{in, min}} )</th>
<th>Long-term maximal input voltage ( U_{\text{in, max}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{Interlock delay time 0.2}(T_{\text{sw}}/2) )</td>
<td>( D_{\text{max}} = 0.4 )</td>
<td>( D_{\text{max}} = 0.22 )</td>
</tr>
<tr>
<td>Switch duty cycle</td>
<td>( D_{\text{max}} = 0.49 )</td>
<td>( D_{\text{max}} = 0.27 )</td>
</tr>
</tbody>
</table>

Impact on the inverter losses

With the extension of the duty cycle values, the rms voltage applied to the transformer’s primary winding will be increased. For the same transferred power, the rms value of the primary current should proportionally decrease. As a consequence, the rms current of the switching transistors will be decreased, which gives a positive impact on the inverter losses. Table 5 presents the comparison of the inverter switch values corresponding to the old (20% from the half period) and the new minimized (2% from the half period) interlock delay time.

Table 5. Impact of the interlock delay time minimization on the operating values of the inverter switches

<table>
<thead>
<tr>
<th>Switch duty cycle</th>
<th>( U_{\text{in, max}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( D_{\text{max}} = 0.4 )</td>
<td>0.22</td>
</tr>
<tr>
<td>( D_{\text{max}} = 0.22 )</td>
<td>12.5</td>
</tr>
<tr>
<td>( D_{\text{max}} = 0.49 )</td>
<td>26.7</td>
</tr>
<tr>
<td>( D_{\text{max}} = 0.27 )</td>
<td>24.1</td>
</tr>
</tbody>
</table>

As seen from Table 5, the rms current of the inverter switches with the extended duty cycle could be 1.1 times lower than with the previous version. Such minimization of rms current results in decreased average losses of the inverter. Fig. 5 depicts the comparison of the losses of a half-bridge inverter operating within different duty cycle ranges. Fig. 5 (a) shows that such minimization of the effective interlock delay time tends to an 8% decreased loss of the inverter at the long-term maximal input voltage. At the long-term maximal input voltage, the losses of the inverter

![Estimated for the long-term maximal input voltage \( U_{\text{in, max}} = 4000 \text{ V} \)]

(a)

![Estimated for the long-term maximal input voltage \( U_{\text{in, max}} = 2200 \text{ V} \)]

(b)
Impact on the isolation transformer

The 90% minimization of the interlock delay time (from \(0.2T_{sw2}\) to 0.02\(T_{sw2}\)) will be followed by the decrease of the amplitude value of the transformer secondary voltage. Neglecting losses in the rectifier diodes and output filter components, the transformer secondary amplitude voltage could be estimated by (6).

\[
U_{sec,amp} = \frac{U_{sec}}{2 \cdot D}
\]

where \(U_{sec}\) is the converter output voltage. Tables 6 and 7 present the results of the impact of the interlock delay time minimization on the main specifications of the isolation transformer.

As shown in Tables 6 and 7, an isolation transformer will undergo several changes, like a 10% increase in the primary rms voltage and about 10% increase in the secondary rms current in the case of minimized interlock delay time. All that will result in two additional turns in the primary and three turns shorter secondary winding. But to compensate the minor changes in the turns number. Thus, the transformer will have the same volume in both cases (for the same magnetic core material, operating flux density and winding material).

Table 6. Main specifications of the isolation transformer estimated for the interlock delay time 0.2\((T_{sw2})\)

<table>
<thead>
<tr>
<th>Boundary operating points</th>
<th>Long-term minimal input voltage (U_{in,mm}) (2.2 kV)</th>
<th>Long-term maximal input voltage (U_{in,max}) (4.0 kV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch duty cycle</td>
<td>(D_{max} = 0.4)</td>
<td>(D_{min} = 0.22)</td>
</tr>
<tr>
<td>Primary amplitude voltage</td>
<td>1.10</td>
<td>2.00</td>
</tr>
<tr>
<td>Primary rms voltage</td>
<td>0.98</td>
<td>1.33</td>
</tr>
<tr>
<td>Primary rms current</td>
<td>50.8</td>
<td>37.7</td>
</tr>
<tr>
<td>Secondary amplitude voltage</td>
<td>0.44</td>
<td>0.80</td>
</tr>
<tr>
<td>Secondary rms voltage</td>
<td>0.39</td>
<td>0.53</td>
</tr>
<tr>
<td>Secondary rms current</td>
<td>127.8</td>
<td>94.8</td>
</tr>
<tr>
<td>Turns ratio</td>
<td>2.51:1</td>
<td>45/18</td>
</tr>
<tr>
<td>Prim./sec. turns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 7. Main specifications of the isolation transformer estimated for the interlock delay time 0.02\((T_{sw2})\)

<table>
<thead>
<tr>
<th>Boundary operating points</th>
<th>Long-term minimal input voltage (U_{in,mm}) (2.2 kV)</th>
<th>Long-term maximal input voltage (U_{in,max}) (4.0 kV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch duty cycle</td>
<td>(D_{max} = 0.49)</td>
<td>(D_{min} = 0.27)</td>
</tr>
<tr>
<td>Primary amplitude voltage</td>
<td>1.10</td>
<td>2.00</td>
</tr>
<tr>
<td>Primary rms voltage</td>
<td>1.09</td>
<td>1.47</td>
</tr>
<tr>
<td>Primary rms current</td>
<td>45.9</td>
<td>34.0</td>
</tr>
<tr>
<td>Secondary amplitude voltage</td>
<td>0.36</td>
<td>0.65</td>
</tr>
<tr>
<td>Secondary rms voltage</td>
<td>0.35</td>
<td>0.48</td>
</tr>
<tr>
<td>Secondary rms current</td>
<td>144.3</td>
<td>104.9</td>
</tr>
<tr>
<td>Turns ratio</td>
<td>3.08:1</td>
<td>46/15</td>
</tr>
</tbody>
</table>

A more interesting fact is derived from the analysis of the fundamental power of the isolation transformer. After the Fourier transformation of the rectangular voltage pulse shape, the fundamental power of the isolation transformer could be evaluated by (7).

\[
P_f = \frac{U_{sec, rms}^2}{R_{ekv}} = \left(\frac{U_{sec, amp}}{\sqrt{2}}\right)^2 \cdot \frac{P}{U_{sec, amp}^2} = \left(\frac{4}{\pi}\right) \frac{P}{U_{sec, amp}^2} \cdot \frac{\sin \pi D}{\sqrt{2}} = 4 \cdot \frac{P}{\pi} \cdot \left(\sin \pi D\right)^2 \cdot \frac{D}{\pi^2},
\]

where \(P\) is the desired power of the isolation transformer and \(D\) is the duty cycle.

According to the standard EN50163, the developed converter must operate normally at the rated load and within the predefined input voltage limits (presented in Table 1). Investigations show that the voltage in the traction catenary is mostly fluctuating within the range of 2.9...3.3 kV (Fig. 7). The nominal voltage in that case is 3.1 kV and it will be a feasible solution to provide more power from the fundamental harmonic exactly at this operating point.

In case the interlock delay time of the inverter switches is selected as 0.2\((T_{sw2})\), the duty cycle variation range is 0.4 to 0.22 at the minimal and the maximal input voltage, correspondingly. The power of the fundamental harmonic will change from 37.4 kVA at \(D_{min}=0.22\) to 45.8 kVA and \(D_{max}=0.4\) (see Fig. 6). The fundamental harmonic power corresponding to the nominal operating point (input voltage \(U_{in, nom}=3.1\) kV, \(D_{oper}=0.28\)) in that case will be 43.3 kVA.

As it was predicted earlier, by the minimization of the interlock delay time from 0.2\((T_{sw2})\) to 0.02\((T_{sw2})\) the power of the fundamental harmonic will change from...
42.2 kVA at $D_{\text{nom}}=0.27$ to 41.3 kVA and $D_{\text{nom}}=0.49$ (see Fig. 8). Moreover, the output power of the fundamental harmonic will be increased by more than 6% at the nominal operating point ($D_{\text{nom}}=0.35$).

Impact on the filters

The output filter capacitance and inductance should be selected according to the maximum and minimum switch duty cycles, correspondingly. It was considered that the output load current, output voltage as well as the accepted output voltage ripple current have the same values in both investigated cases.

Fig. 10 shows the relationship between the minimum duty cycle and the minimum inductance requirements of the output filter to ensure a 5% peak-to-peak current ripple on the output inductor. The minimization of the interlock delay time will be followed with the increase of the switch duty cycle at the boundary operation points, which in turn will lead to smaller inductance required to ensure proper ripple current. Thus, the proposed 90% reduction of the interlock delay will lead to a 20% reduced demand on the filtering inductance.

Results from the study of the minimum capacitance required for the output filter to ensure the accepted 5% voltage ripple on the output showed that a 90% decrease in the interlock delay time, which, in turn, leads to a proportional increase in the transistor conduction time, will both lead to a 20% increase in the filtering capacitor demand (Fig. 11).
Fig. 11. Relation between the maximum duty cycle and the minimum required capacitance of an output filter

From the practical viewpoint, the 20% reduction of the required inductance will lead to an 11.5% decreased turn number of the filtering inductor for the same operating power. It must be mentioned that the output inductor is conducting a high current (up to 142 A at the rated load) and even minor changes in the number of turns give a positive impact on the power losses of it.

On the other hand, a rise in the required capacitance as a consequence of the minimized interlock delay time could be easily solved by the implementation of more powerful capacitors and with no serious impact on the occupied space and overall feasibility.

Conclusions

Focus in this paper is on the analysis of minimization possibilities of the interlock delay time in the half-bridge high-voltage IGBT based high-power converter. It is shown that the effective delay time between switching on the top and bottom arm transistors in the half-bridge configuration could be decreased from the recently recommended 20% of the half period to a 2% of the half period with no effect on the inverter reliability. Such progressive minimization of the interlock delay will in turn increase the transistor on-state time.

The second part of the paper is devoted to the analysis of the impact of the delay time minimization on the converter components, efficiency and overall feasibility. The results show that the 90% minimization of the interlock delay time will be followed by a 7% lower power dissipation of the high-voltage half-bridge inverter, better power transfer of the isolation transformer, especially at the nominal operating point. Moreover, the inductance of the output inductor could be reduced by 20%, which results in lower power dissipation and reduced weight and volume due to a smaller quantity of copper used in the winding.

Despite a number of benefits gained by the discussed minimization of the interlock delay time, the selection of a proper minimum delay should be performed very carefully. In general, theoretical evaluations concerning the minimum dead time based on the component datasheet should be always followed by the measurements of the switching properties of the IGBTs and signal propagation delays of the control system. Otherwise, an improper selection of the interlock delay could cause the short circuit of the input side of the converter, usually with disastrous results.

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